AMENDMENTS TO THE CLAIMS

Please cancel claims 2, 7-11, 13, and 15-20 without prejudice or disclaimer of their underlying subject matter.

1-20 (canceled)

Please add the following new claims.

21. (new) A semiconductor package comprising:

a first insulating substrate having a first surface and a second surface opposite said first surface, said first surface having electrically conductive patterns and electrically conductive pattern lands formed thereon, said second surface having a heat dissipating pattern and second surface lands formed thereon;

a heat radiating plate that radiates heat from within said semiconductor device, said heat dissipating pattern and said second surface lands being between said first insulating substrate and said heat radiating plate;

a semiconductor device bonded onto said first surface, bond wires connecting said semiconductor device to said electrically conductive patterns, said electrically conductive patterns being connected to said electrically conductive pattern lands;

a sidewall section on said first surface, said sidewall section encircling said semiconductor device, a cavity being a concave shape defined by said first insulating substrate and said sidewall section, said semiconductor device being contained within said cavity;

a second insulating substrate covering said sidewall section and said cavity, said second insulating substrate having a through-hole land portion and a solder land portion, said through-hole land portion being disposed at the rim of said second insulating substrate to contact said sidewall section, and a solder land portion being disposed at the central part of said second insulating substrate to contact said cavity;

through-hole lands disposed at said through-hole land portion;

solder lands disposed at said solder land portion;

conductor patterns connecting said solder lands to said through-hole lands; and

through-holes extending from said through-hole lands, through said second insulating substrate, said sidewall section, said electrically conductive pattern lands, said first surface, and said second surface, to said second surface lands, said through-holes being plated to form plated through-holes.

22. (new) A semiconductor package according to claim 21 wherein said through-hole lands and said solder lands are on a surface of said second insulating substrate.

23. (new) A semiconductor package according to claim 21 wherein said through-hole lands contact said plated through-holes.

24. (new) A semiconductor package according to claim 21 wherein an adhesive between said first insulating substrate and said heat radiating plate bonds said first insulating substrate to said heat radiating plate.

25. (new) A semiconductor package according to claim 21 wherein said semiconductor device is bonded onto said first surface using a thermosetting adhesive.

26. (new) A semiconductor package according to claim 21 wherein said first insulating substrate comprises a glass cloth impregnated with an epoxy resin.

27. (new) A semiconductor package according to claim 21 wherein said second insulating substrate comprises a glass cloth impregnated with an epoxy resin.

28. (new) A semiconductor package according to claim 21 wherein said electrically conductive patterns are disposed circumferentially about said semiconductor device.

29. (new) A semiconductor package according to claim 21 wherein said sidewall section includes a prepreg layer and a spacer substrate.

30. (new) A semiconductor package according to claim 21 wherein a prepreg layer is disposed between said second insulating substrate and said sidewall section.

31. (new) A semiconductor package according to claim 21 wherein said first insulating substrate is a laminated sheet lined with copper on said first and second surfaces, said copper on said first surface forming said electrically conductive patterns and said electrically conductive pattern lands, said copper on said second surface forming said through-hole lands and said solder lands.

32. (new) A semiconductor package according to claim 21 wherein said solder lands are formed on second insulating substrate as a lattice.

33. (new) A semiconductor package according to claim 21 wherein one of said solder lands is interconnected to only one of said through-hole lands.

34. (new) A semiconductor package according to claim 33 wherein said through-hole lands are disposed only at said through-hole land portion.

35. (new) A semiconductor package according to claim 21 wherein an encapsulating resin encases said semiconductor device.

36. (new) A semiconductor package according to claim 35 wherein said encapsulating resin fills said cavity.

37. (new) A semiconductor package according to claim 35 wherein said encapsulating resin is co-planar with said sidewall section.

38. (new) A semiconductor package according to claim 37 wherein said encapsulating resin is planarized.

39. (new) A method for the preparation of a semiconductor package comprising the steps of:

forming electrically conductive patterns and electrically conductive pattern lands on a first surface of a first insulating substrate;

forming a heat radiating plate that radiates heat from within said semiconductor device, said heat dissipating pattern and said second surface lands being between said first insulating substrate and said heat radiating plate;

bonding a semiconductor device onto said first surface;

connecting said semiconductor device to said electrically conductive patterns with bond wires;

connecting said electrically conductive patterns to said electrically conductive pattern lands;

encircling said semiconductor device with a sidewall section to form a cavity, said sidewall section being formed on said first surface, said cavity being a concave shape defined by

said first insulating substrate and said sidewall section, said semiconductor device being contained within said cavity;

covering said sidewall section and said cavity with a second insulating substrate, said second insulating substrate having a through-hole land portion and a solder land portion, said through-hole land portion being disposed at the rim of said second insulating substrate to contact said sidewall section, and a solder land portion being disposed at the central part of said second insulating substrate to contact said cavity;

extending through-holes through said second insulating substrate, said sidewall section, said electrically conductive pattern lands, said first surface, and said second surface, to said second surface lands, said through-holes being plated to form plated through-holes;

forming through-hole lands at said through-hole land portion, said through-hole lands contacting said plated through-holes;

forming solder lands at said solder land portion; and

connecting said solder lands to said through-hole lands with conductor patterns.

40. (new) A method for the preparation of a semiconductor package according to claim 39 wherein said through-hole lands and said solder lands are formed on a surface of said second insulating substrate.

41. (new) A method for the preparation of a semiconductor package according to claim 39 further comprising the step of:

forming an adhesive between said first insulating substrate and said heat radiating plate to bond said first insulating substrate to said heat radiating plate.

42. (new) A method for the preparation of a semiconductor package according to claim 39 further comprising the step of:

bonding said semiconductor device onto said first surface using a thermosetting adhesive.

43. (new) A method for the preparation of a semiconductor package according to claim 39 wherein said first insulating substrate comprises a glass cloth impregnated with an epoxy resin.

44. (new) A method for the preparation of a semiconductor package according to claim 39 wherein said second insulating substrate comprises a glass cloth impregnated with an epoxy resin.

45. (new) A method for the preparation of a semiconductor package according to claim 39 wherein said electrically conductive patterns are disposed circumferentially about said semiconductor device.

46. (new) A method for the preparation of a semiconductor package according to claim 39 wherein said sidewall section includes a prepreg layer and a spacer substrate.

47. (new) A method for the preparation of a semiconductor package according to claim 39 wherein a prepreg layer is disposed between said second insulating substrate and said sidewall section.

48. (new) A method for the preparation of a semiconductor package according to claim 39 wherein said first insulating substrate is a laminated sheet lined with copper on said first and second surfaces, said copper on said first surface forming said electrically conductive patterns and said electrically conductive pattern lands, said copper on said second surface forming said through-hole lands and said solder lands.

49. (new) A method for the preparation of a semiconductor package according to claim 39 wherein said solder lands are formed on second insulating substrate as a lattice.

50. (new) A method for the preparation of a semiconductor package according to claim 39 wherein one of said solder lands is interconnected to only one of said through-hole lands.

51. (new) A method for the preparation of a semiconductor package according to claim 50 wherein said through-hole lands are disposed only at said through-hole land portion.

52. (new) A method for the preparation of a semiconductor package according to claim 39 further comprising the step of:

encasing said semiconductor device with an encapsulating resin.

53. (new) A method for the preparation of a semiconductor package according to claim 52 wherein said encapsulating resin fills said cavity.

54. (new) A method for the preparation of a semiconductor package according to claim 52 further comprising the step of:

planarizing said encapsulating resin.

55. (new) A method for the preparation of a semiconductor package according to claim 52 wherein said encapsulating resin is co-planar with said sidewall section.